Log-Domain Time-Multiplexed Realization of Dynamical Conductance-Based Synapses

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***Abstract*—We present a compact circuit architecture for analog VLSI realization of event-addressable neuromorphic arrays with conductance-based synaptic dynamics. Synaptic input events are time-multiplexed, pooled by synapse type according to common reversal potential and activation dynamics. One such physical synapse element per postsynaptic neuron is provided for each type, selected by type index along with postsynaptic address. A log-domain encoding of first-order linear dynamics of synaptic conductance results in a compact circuit realization with three MOS transistors per synapse element. Circuit simulations show low-power operation with linear dynamics in conductance.**

I. Introduction

Neuromorphic engineering [1] utilizes inspiration from biology and neurobiology to direct and motivate the design and modeling of circuits and systems. By emulating form and architecture in biological systems, neuromorphic engineering seeks to emulate function as well. Investigation of neural behavior on large scale requires efficient and realistic modeling and implementation of neurons and their synaptic connections [2]-[4].

Analysis of a variety of different implementations of conductance-based dynamical synapses, and new circuit that overcomes some of their limitations, are presented in [5]. In particular, [5] analyzes the trade-offs among the different implementations regarding functionality of the temporal dynamics and the required layout size, and offers a circuit with linear dynamics in conductance. Earlier implementations of VLSI synapses such as the pulse current-source synapse [1] and reset-and-discharge synapse [6] suffer from inability to integrate input spikes into continuous output currents and linearly sum postsynaptic currents respectively. Other previous circuits such as the linear charge-and-discharge synapse [7] and current-mirror-integrator synapse [8], [9] , and [10] also suffer from nonlinear summation of postsynaptic currents. The synapse implementations of log-domain integrator synapse [11] and diff-pair integrator synapse [5] implement linear summation of postsynaptic currents, but they require an M_w p-FET or additional transistors.

Here we show that a variant on the log-domain implementation gives rise to linear conductance dynamics in more compact form. Here we present a three-transistor realization of a dynamical conductance-based synapse element, serving multiple synapses with common reversal potential and activation dynamics. The time-multiplexing synapse element pools spike input events from multiple presynaptic source addresses through the address-event representation (AER, [12]) communication framework as seen in Fig. 1.

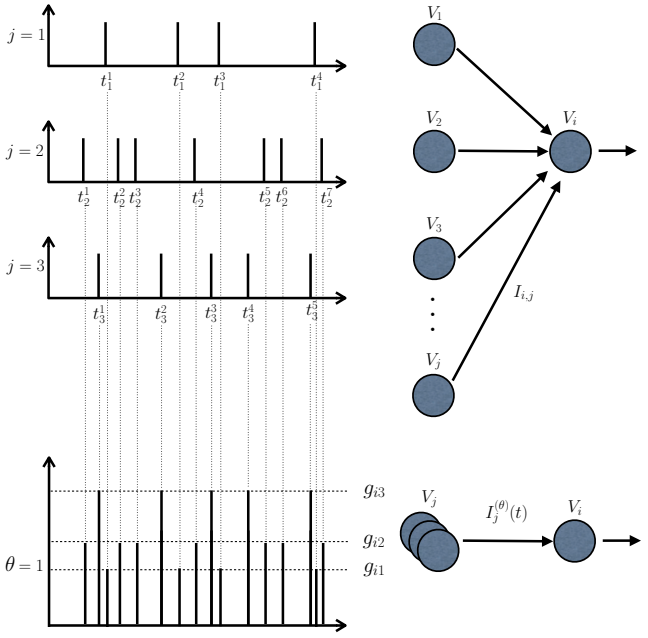

Fig. 1. Pooling of synapses with common reversal potential and activation dynamics, but possibly with different conductances, by time-multiplexing input events from j presynaptic neurons.

II. Synapse Array Architecture

This paper focuses upon the architectural design of the pooled synapse input for each neuron within the neural array. We assume that the number of *distinct* synapse types is limited to a relatively low number k, *e.g.*, $k = 8$. This assumption is typically valid even in large-scale cortical models. We pool synapses of the same type serving the same postsynaptic terminal into a time-multiplexed synapse element. Synapse elements in the array are activated by presynaptic events presented through an AER input interface [12]. Neurons receiving

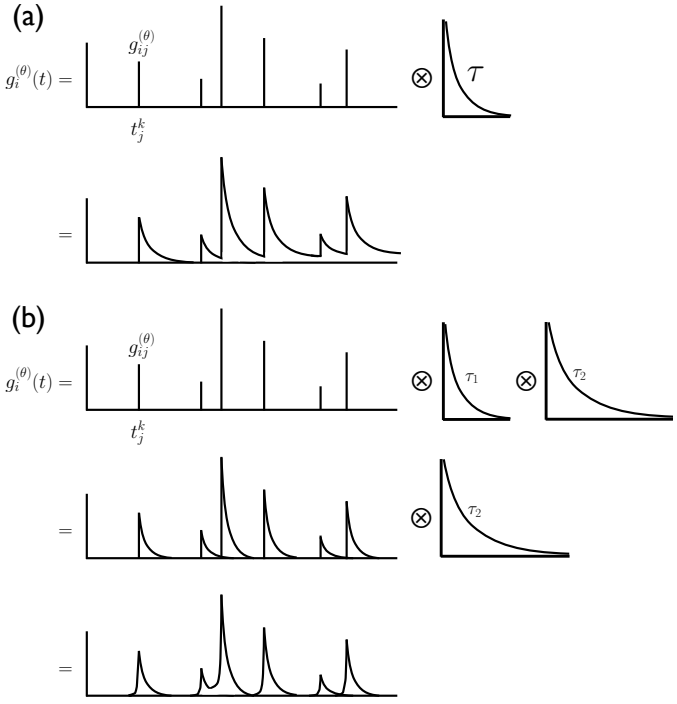

Fig. 2. Illustration of the convolution between the conductance dynamics and conductance strength using two versions (a) a single decay τ, and (b) a rise and fall time τ_1 and τ_2.

synaptic inputs from these elements further interface through AER arbitration to generate postsynaptic output events [12].

III. Synapse Element

A. Modeling of Conductance Dynamics

We assume a general conductance-based synapse with continuous activation dynamics. The postsynaptic membrane receives synaptic current contributions,

$$\sum_j I_{ij} = \sum_j \sum_k g_{ij} f_{ij}(t - t_j^k)(V_i - E_{ij}) \tag{1}$$

where i denotes the post-synaptic neuron, j denotes the pre-synaptic neuron, k indicates the spiking event number, g_{ij} is the conductance strength between neuron i and neuron j, $f_{ij}(t - t_j^k)$ indicates the conductance dynamics profile, V_i is the membrane voltage of pre-synaptic neuron i, and E_{ij} is the reversal potential between neuron i and neuron j.

Synaptic current contributions to postsynaptic neuron i are partitioned according to synapse type as

$$\sum_j I_{ij} = \sum_j {I_{ij}}^{(1)} + \sum_j {I_{ij}}^{(2)} + \ldots + \sum_j {I_{ij}}^{(k)} \tag{2}$$

where each partition serves synapses with common synapse parameters in terms of reversal potentials

$$E_{ij}^{(\theta)} = E^{(\theta)} \ \forall \ i, j \tag{3}$$

and activation dynamics

$$f_{ij}^{(\theta)} = f^{(\theta)} \ \forall \ i, j \tag{4}$$

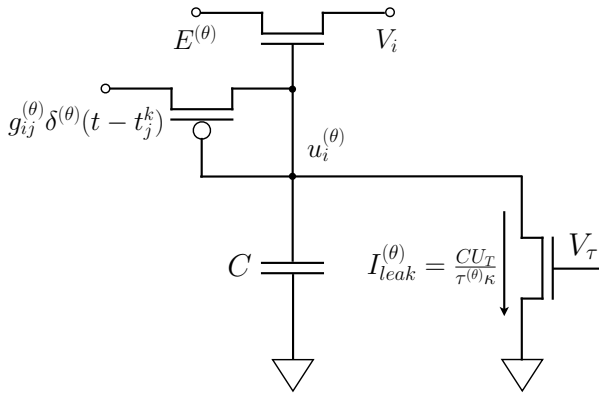

Fig. 3. The circuit implementing the synapse element consisting of 3 MOS transistors.

where θ indicates the synapse type. The partitions pool each of the synaptic contributions from the respective presynaptic neurons as:

$$\begin{aligned} \sum_j I_{ij}^{(\theta)} &= \sum_\theta \sum_j \sum_k g_{ij}^{(\theta)} f^{(\theta)}(t - t_j^k)(V_i - E^{(\theta)}) \\ &= \sum_\theta \sum_k g_i^{(\theta)}(t)(V_i - E^{(\theta)}) \end{aligned} \tag{5}$$

where $g_i^{(\theta)}(t)$ denotes the time-multiplexed pooled conductance of synapse element (θ) of postsynaptic neuron i:

$$g_i^{(\theta)}(t) = \sum_j g_{ij}^{(\theta)} f^{(\theta)}(t - t_j^k). \tag{6}$$

The temporal profile of $g_i^{(\theta)}(t)$ is illustrated in Fig. 2. A log-domain recurrence relation expressing this pooled conductance leads to compact realization as described next.

B. Linear and Log-Domain Recurrence Relation

A general conductance dynamics profile $f^{(\theta)}$ can be characterized by two terms: a fall time $\tau_1^{(\theta)}$ and a rise time $\tau_2^{(\theta)}$. We start by modeling the transient conductance dynamics as a single decaying exponential with time constant $\tau^{(\theta)}$ as illustrated in Fig. 2(a), and note that the more general case can be implemented by convolution of the activation functions $g_{ij}^{(\theta)}$ with decaying exponential on shorter time scale as illustrated in Fig. 2(b). The convolution between the conductance dynamics and conductance strength using a single delay $\tau^{(\theta)}$ is expressed as:

$$(\tau^{(\theta)} \frac{d}{dt} + 1) g_i^{(\theta)}(t) = \sum_j g_{ij}^{(\theta)} \delta(t - t_j^k) \tag{7}$$

where $\delta(t - t_j^k)$ is an impulse centered at time t_j^k, representing a presynaptic input event from neuron j of synapse type θ to postsynaptic neuron j.

We utilize a log-domain circuit to exploit the linear relationship between the subthreshold MOSFET gate-source voltage

and channel currents. So we express $g_i^{(\theta)}$ in the log-domain:

$$u_i^{(\theta)} = \log g_i^{(\theta)}(t) \quad (8)$$

$$\frac{d}{dt}u_i^{(\theta)} = \frac{1}{g_i^{(\theta)}(t)}\frac{d}{dt}g_i^{(\theta)}(t) \quad (9)$$

leading to

$$\tau^{(\theta)}\frac{d}{dt}u_i^{(\theta)} + 1 = \sum_j \frac{g_{ij}^{(\theta)}(t)}{g_i^{(\theta)}(t)}\delta(t - t_j^k). \quad (10)$$

The solution to the integrator with constant delay (10) in between events t_j^k and t_j^{k+1} is:

$$u_i^{(\theta)}(t) = u_i^{(\theta)}(t_j^k) - \frac{t - t_j^k}{\tau^{(\theta)}}\ ,\ t_j^k < t < t_j^{k+1} \quad (11)$$

and at the arrival of an event t_j^k, for $\epsilon \to 0$:

$$u_i^{(\theta)}(t_j^k + \epsilon) = u_i^{(\theta)}(t_j^k - \epsilon) + g_{ij}^{(\theta)}e^{-u_i^{(\theta)}(t_j^k - \epsilon)}. \quad (12)$$

Transformed back to the current domain, the resulting conductance $g_i^{(\theta)}$ follows the desired linear dynamics in input activation:

$$g_i^{(\theta)}(t_j^k + \epsilon) = g_i^{(\theta)}(t_j^k - \epsilon) + g_{ij}^{(\theta)} \quad (13)$$

and exponential decaying conductance in between presynaptic events with time constant:

$$g_i^{(\theta)}(t) = g_i^{(\theta)}(t_j^k)e^{-(t - t_j^k)/\tau^{(\theta)}}\ ,\ t_j^k < t < t_j^{k+1}. \quad (14)$$

IV. Circuit Architecture

The common reversal potential parameter for each synapse partition $E^{(\theta)}$ is simply implemented as a single nMOS transistor operating in the subthreshold region:

$$I_{NMOS} = \lambda I_0 e^{\kappa_n V_g/U_T}(e^{-V_s/U_T} - e^{-V_d/U_T}), \quad (15)$$

where V_g is the gate voltage, V_s is the source voltage, V_d is the drain voltage, λ is the W/L ratio of the transistor, I_0 is the subthreshold pre-exponential current factor, κ_n indicates the back gate effect, and U_T is the thermal voltage, kT/q. The transistor operates in the subthreshold region while the drain-to-source voltage is less than $4U_T$. Since the voltages are implemented in log-domain circuits, the resulting output current can be expressed as:

$$I \propto \kappa V_u(V_i - E^{(\theta)}), \quad (16)$$

To implement the input recurrence (12) composed of the input term of the incoming conductance strength value $g_{ij}^{(\theta)}$ multiplied by a negative exponential $e^{-u_i^{(\theta)}(t_j^k)}$, we utilize CMOS technology to implement the negative exponential $e^{-u_i^{(\theta)}(t_j^k)}$ with a single diode-connected pMOS transistor operating in the subthreshold region:

$$I_{PMOS} \propto e^{-\kappa_p V_g/U_T}, \quad (17)$$

We activate the pMOS with a short pulse centered at t_j^k. The conductance strength $g_{ij}^{(\theta)}$ can in principle be implemented by modulating the pulse voltage logarithmically. Rather than adding this complication to the circuit and the drivers at the periphery of the array, we modulate the pulse width linearly in the conductance strength $g_{ij}^{(\theta)}$. Notice that a back gate effect parameter κ_n and κ_p is present in both of the expressions for the input (13) and output (15) of the synapse element. The κ parameter indicates the efficiency of a change the gate voltage and the resultant change in surface potential. This loss in efficiency is due to the bulk terminal in a MOSFET, which can act as another gate terminal (also referred to as the 'back-gate effect'). Fortunately, this effect will have little consequence if the nMOS and pMOS devices have sufficiently close back-gate effects, $\kappa_n \approx \kappa_p$.

By virtue of the log-domain transformation, the decaying exponentials $e^{-t/\tau}$ in the conductance dynamics $f_{ij}(t - t_j^k)$ are implemented using a single nMOS transistor operated in

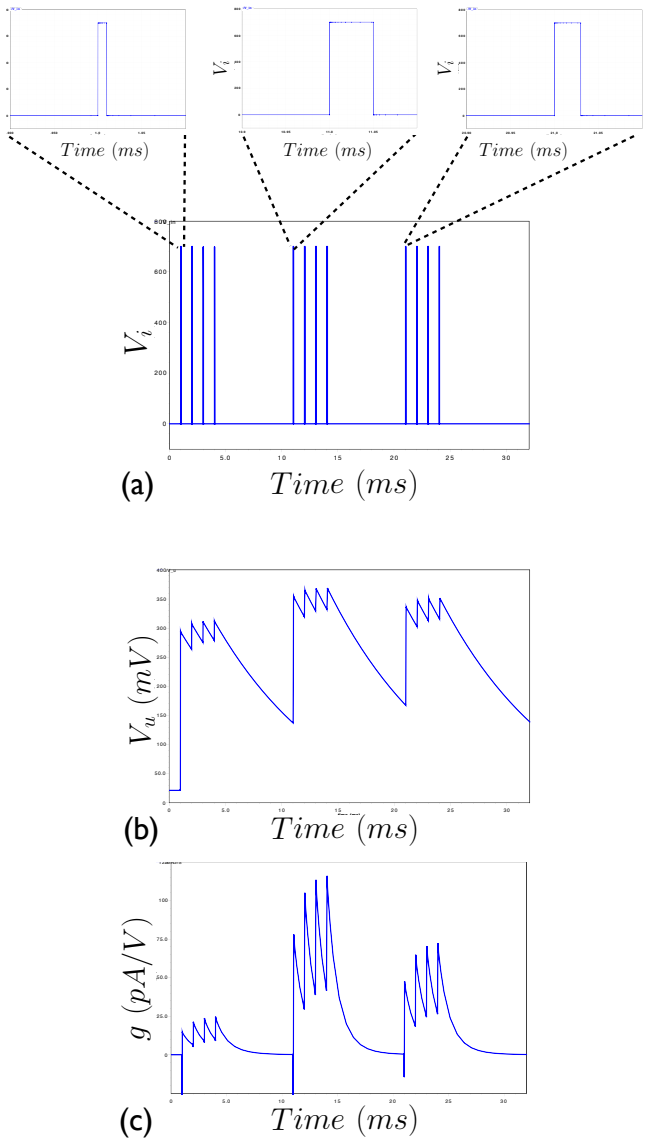

Fig. 4. Transistor-level circuit simulation illustrating both the: a) activation function $g_i^{(\theta)}$ with 3 groups of different activation widths (detail shown in inset); b) log-domain variable u and c) time-domain conductance g.

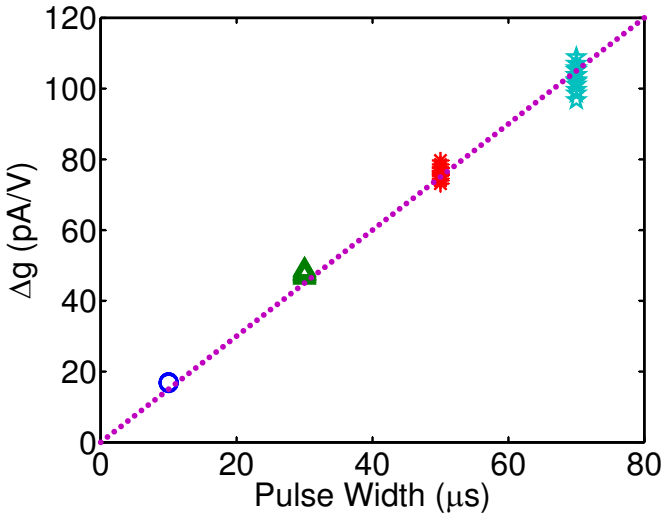

Fig. 5. Transistor-level circuit simulation illustrating Δg for 4 groups of different activation widths.

subthreshold and used as a constant current source to linearly charge capacitor C. As shown in Fig. 2(b), the conductance dynamics $f_{ij}(t - t_j^k)$ can be extended to a rise time τ_1 and fall time τ_2 through convolution. This could be accomplished by driving the source of the pMOS with a sequence of pulses. The complete dynamical conductance-based synapse circuit implementation is shown in Fig. 3. The circuit is compact, requiring only 3 transistors to implement.

V. Characterization

To verify the conductance dynamics, we performed transistor-level simulations (using Spectre and parameters of a 0.13μm CMOS process) of the synapse circuit driven by a train of presynaptic impulses, modulated with three different pulse widths, with relative magnitudes 1, 3, and 5, emulating the effect of three time-multiplexed pooled synapses. The circuit output in response to the sequence of input synaptic events is shown in Fig. 4.

To verify the linearity of postsynaptic conductance in presynaptic activation, we studied the dependence of the conductance time profile as a function of pulse width and pulse interval. We observed the step in conductance Δg for a train of pulses at variable pulse intervals, for four different values of pulse width with relative magnitudes 1, 3, 5, and 7 as shown in Fig. 5. The four distinct and compact groups for each of the four different activation widths indicate the linearity of the conductance according to the convolution model (13) and (14). Furthermore, the centers of the clusters for each of the different activation widths are colinear through the origin, confirming linearity in input pulse width.

VI. Conclusion

We have formulated a dynamical conductance-based synapse cell in a compact circuit design. Circuit simulations verify log-domain implementation as well as an output magnitude scaled to the input conductance strength. The circuit implementation is compact, requiring only 3 transistors. This small footprint, coupled with the low-power subthreshold design, make this design a suitable candidate for large-scale implementation of synaptic arrays in addressable neuromorphic systems, with reconfigurable synaptic connectivity as well as individually selectable synaptic dynamics.

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